WHAT IS CLAIMED IS:

1. An adaptive clock throttle for interfacing a clock generator generating a high speed clock and a processing engine operating in response to a processing clock, the adaptive clock throttle operable to:

generate a plurality of lower speed clocks from the high speed clock;

estimate a duty cycle of the processing engine; and

selectively gate one of the lower speed clocks to the processing engine as the processing clock to increase the duty cycle of the processing engine.

2. The adaptive clock throttle of Claim 1 further operable to selectively mask the selected lower speed clock to produce a series of non-periodic clock cycles.

3. The adaptive clock throttle of Claim 2 wherein the adaptive clock throttle is operable to mask the selected lower speed clock in predetermined pattern.

4. The adaptive clock throttle of Claim 2 wherein the adaptive clock throttle is operable to pseudorandomly mask the selected lower speed clock.

5. The adaptive clock throttle of Claim 1 wherein the processing engine comprises a digital signal processor.

6. The adaptive clock throttle of Claim 1 wherein at least one of the lower speed clocks is asymmetric.

7. The adaptive clock throttle of Claim 1 further operable to:

monitor the status of an output data buffer of the processing engine;

detect an underflow condition in the buffer; and

selectively gate one of the high and lower speed clocks to the processing engine to increase the processing engine operating frequency in response to the underflow condition.

8. The adaptive clock throttle of Claim 1 further operable to:

monitor the status of a data buffer of the processing engine;

detect an underflow condition in the buffer; and

selectively remask the selected lower speed clock to increase the processing engine operating frequency in response to the underflow condition.

9. A method of reducing noise in a single-chip system including at least one processor operating on data as blocks in response to a set of instructions, the method comprising the steps of:

processing a selected block with the processor in response to a processor clock of a selected frequency;

during the processing of the selected block of data, estimating the processor loading; and

in response to said step of estimating the processor loading, selectively changing the frequency of the processor clock to more uniformly distribute the processor loading across the processing period of a block.

10. The method of Claim 9 wherein said step of estimating the processor loading comprises the substeps of:

for a selected number of clock periods during the processing of the selected block, counting a number of active clock cycles during which an instruction is executed and a number of sleep clock cycles during which instructions are not executed; and

estimating a duty cycle proportional to the processor load from the ratio of the active clock cycles to the sleep clock cycles.

11. The method of Claim 9 wherein said step of changing the frequency of the processor clock comprises the substep of:

generating a plurality of clocks of varying frequencies; and

gating a selected one of the plurality of clocks to the processor as the processor clock.

12. The method of Claim 9 wherein said step of changing the frequency of the processor clock comprises the substep of selectively masking active edges of the processor clock.

13. The method of Claim 12 wherein said substep of selectively masking comprises the substep of pseudorandomly masking active edges of the clock.

14. The method of Claim 9 and further comprising the steps of:

detecting a data underflow condition in the processor; and

selectively increasing the frequency of the processor clock in response to the underflow condition.

15. The method of Claim 14 wherein said step of detecting a data underflow condition comprises the substep of monitoring a dipstick associated with a data buffer in the processor.

16. An audio decoder for operating on audio data received in blocks comprising:

a digital signal processor for processing blocks of audio data in response to a set of instructions;

clock generation circuitry operable to generate a plurality of clocks; and

an adaptive clock throttle interfacing the digital signal processor and the clock generation circuitry operable to:

estimate the loading on the digital signal processor as the processor executes instructions to process the blocks of audio data; and

selectively gate one of the plurality of clocks to the processor as a function of the estimated loading for timing processor operations, the clock selected to distribute the execution of instructions for a selected block of audio data across a period of the selected block.

17. The audio decoder of Claim 16 wherein the digital signal processor is a selected one of a plurality of digital signal processors integrated on a single-chip.

18. The audio decoder of Claim 16 wherein the adaptive clock throttle is further operable to selectively mask periods of the selected clock to change a frequency of the selected clock.

19. The audio decoder of Claim 16 wherein the clock generator is operable to generate at least one of the plurality of clocks as an asymmetric clock.

20. The audio decoder of Claim 16 wherein the clock generator is operable to generate the plurality of clocks from a high speed clock.